Claims

We claim:

1. A semiconductor memory, comprising:

a first capacitor for storing digital data connecting a cell plate line to a first bit-line through a first select transistor, the first select transistor activated through a connection to a word line;

at least one reference capacitor for providing a reference voltage to a reference bit-line;

a sense amplifier connected to the first and reference bit-lines for measuring a differential read signal on the first and reference bit-lines; and

a toggle flip flop for alternately changing polarization of charge stored on the at least one reference capacitor.

2. The semiconductor memory of Claim 1, wherein the at least one reference capacitor includes two reference capacitors, each one alternating between serving as a switching reference capacitor and a non-switching reference capacitor.

3. The semiconductor memory of Claim 2, wherein the reference capacitors are ferroelectric capacitors.

4. The semiconductor memory of Claim 3, wherein the first capacitor is also a ferroelectric capacitor.

5. The semiconductor memory of Claim 1, wherein the toggle flip flop is comprised of NAND gates.

6. The semiconductor memory of Claim 2, wherein the toggle flip flop alternately changes the polarization of the charge stored on the at least one reference capacitor by toggling write back signals supplied to the two reference capacitors.

7. The semiconductor memory of Claim 6, wherein the charges on the two reference capacitors are averaged to supply the reference voltages to the sense amplifier.

8. The semiconductor memory of Claim 1, wherein the first capacitor for storing digital data is part of a 1T1C memory cell.

9. The semiconductor memory of Claim 1, wherein the at least one reference capacitor is part a cell also including a transistor, and wherein multiple such cells are connected in parallel to connect the cell plate line to the first bit-line through the first select transistor.